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E. Willis
10-26-00

PATENT

S/N Unknown

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Wendell P. Noble et al. Examiner: Unknown
Serial No.: Unknown Group Art Unit: Unknown
Filed: Herewith Docket: 303.379US2
Title: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

INFORMATION DISCLOSURE STATEMENT

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for review in connection with the above-identified patent application. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner be returned to the Applicants.

In accordance with 37 C.F.R. § 1.98(d), copies of the listed documents are not provided as these references were previously cited by or submitted to the U.S. Patent Office in connection with Applicants' prior U.S. application, Serial No. 08/939,742, filed on October 6, 1997, which is relied upon for an earlier filing date under 35 U.S.C. §120.

Applicants respectfully request consideration of these references during prosecution of the above-identified matter. The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

WENDELL P. NOBLE ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6904

Date April 17, 2000 By Daniel J. Kluth
Daniel J. Kluth
Reg. No. 32,146